DDR2 SDRAM SODIMM

MT16HTF12864H(I) – 1GB
MT16HTF25664H(I) – 2GB

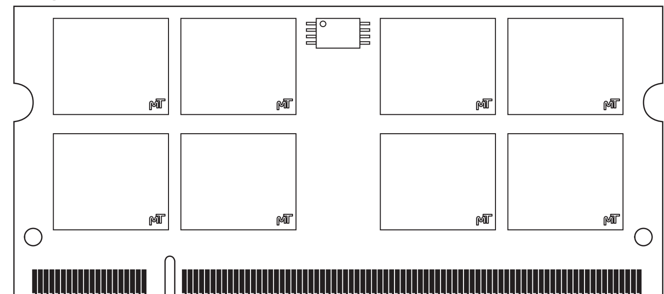
For component data sheets, refer to Micron's Web site: www.micron.com/products/dram/ddr2

Features

- 200-pin, small outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400.
- 1GB (128 Meg x 64), 2GB (256 Meg x 64)
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank

Figure 1: 200-pin SODIMM (MO-224 R/C "B")

Height 30mm (1.18in)



Options | Marking

Options	Marking
• Operating temperature	
• Commercial ($0°C \le T_C \le +85°C$)	
• Industrial ($-40°C \le T_C \le +95°C$)[1,2]	I
• Package	
– 200-pin SODIMM (lead-free)	Y
• Frequency/CAS Latency[3]	
– 2.5ns @ CL = 5 (DDR2-800)	-80E
– 2.5ns @ CL = 6 (DDR2-800)	-800
– 3ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E
– 5.0ns @ CL = 3 (DDR2-400)	-40E
• PCB Height	
– 30mm (1.18in)	

Notes: 1. Industrial operating temperatures apply to DRAM only.
2. Contact Micron for product availability.
3. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–		533	400	15	15	55
-40E	PC2-3200	–		400	400	15	15	55

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Table 2: Addressing

	1GB	2GB
Refresh count	8K	8K
Row address	16K (A0–A13)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device page size per bank	1KB	1KB
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H64M8, 512Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT16HTF12864H(I)Y-80E__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16HTF12864H(I)Y-800__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT16HTF12864H(I)Y-667__	1GB	128 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTF12864H(I)Y-53E__	1GB	128 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTF12864H(I)Y-40E__	1GB	128 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT47H128M8, 1Gb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT16HTF25664H(I)Y-80E__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16HTF25664H(I)Y-800__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT16HTF25664H(I)Y-667__	2GB	256 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTF25664H(I)Y-53E__	2GB	256 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTF25664H(I)Y-40E__	2GB	256 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16HTF12864H(I)Y-40EC2.
2. For the latest component data sheets, see Micron's Web site: www.micron.com/products/dram/ddr2.

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Module Pin Assignments and Descriptions

Table 5: Pin Assignments

200-Pin SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQS2	101	A1	151	DQ42
3	VSS	53	VSS	103	VDD	153	DQ43
5	DQ0	55	DQ18	105	A10/AP	155	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48
9	VSS	59	VSS	109	WE#	159	DQ49
11	DQS0#	61	DQ24	111	VDD	161	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC
15	VSS	65	VSS	115	S1#	165	VSS
17	DQ2	67	DM3	117	VDD	167	DQS6#
19	DQ3	69	NC	119	ODT1	169	DQS6
21	VSS	71	VSS	121	VSS	171	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50
25	DQ9	75	DQ27	125	DQ33	175	DQ51
27	VSS	77	VSS	127	VSS	177	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
31	DQS1	81	VDD	131	DQS4	181	DQ57
33	VSS	83	NC	133	VSS	183	VSS
35	DQ10	85	NC/BA2	135	DQ34	185	DM7
37	DQ11	87	VDD	137	DQ35	187	VSS
39	VSS	89	A12	139	VSS	189	DQ58
41	VSS	91	A9	141	DQ40	191	DQ59
43	DQ16	93	A8	143	DQ41	193	VSS
45	DQ17	95	VDD	145	VSS	195	SDA
47	VSS	97	A5	147	DM5	197	SCL
49	DQS2#	99	A3	149	VSS	199	VDDSPD

200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VSS	52	DM2	102	A0	152	DQ46
4	DQ4	54	VSS	104	VDD	154	DQ47
6	DQ5	56	DQ22	106	BA1	156	VSS
8	VSS	58	DQ23	108	RAS#	158	DQ52
10	DM0	60	VSS	110	S0#	160	DQ53
12	VSS	62	DQ28	112	VDD	162	VSS
14	DQ6	64	DQ29	114	ODT0	164	CK1
16	DQ7	66	VSS	116	A13	166	CK1#
18	VSS	68	DQS3#	118	VDD	168	VSS
20	DQ12	70	DQS3	120	NC	170	DM6
22	DQ13	72	VSS	122	VSS	172	VSS
24	VSS	74	DQ30	124	DQ36	174	DQ54
26	DM1	76	DQ31	126	DQ37	176	DQ55
28	VSS	78	VSS	128	VSS	178	VSS
30	CK0	80	CKE1	130	DM4	180	DQ60
32	CK0#	82	VDD	132	VSS	182	DQ61
34	VSS	84	NC	134	DQ38	184	VSS
36	DQ14	86	NC	136	DQ39	186	DQS7#
38	DQ15	88	VDD	138	VSS	188	DQS7
40	VSS	90	A11	140	DQ44	190	VSS
42	VSS	92	A7	142	DQ45	192	DQ62
44	DQ20	94	A6	144	VSS	194	DQ63
46	DQ21	96	VDD	146	DQS5#	196	VSS
48	VSS	98	A4	148	DQS5	198	SA0
50	NC	100	A2	150	VSS	200	SA1

Notes: 1. Pin 85 is NC for 1GB, BA2 for 2GB.

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Table 6: Pin Descriptions

Symbol	Type	Description
ODT0, ODT1	Input	**On-die termination**: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
CK0, CK0# CK1, CK1#	Input	**Clock**: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input	**Clock enable**: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE power-down and self refresh operations (all device banks idle), or ACTIVE power-down (row ACTIVE in any device bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation V_{REF} must be maintained to this input.
S0#, S1#	Input	**Chip select**: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
RAS#, CAS#, WE#	Input	**Command inputs**: RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0, BA1 (1GB) BA0–BA2 (2GB)	Input	**Bank address inputs**: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
A0–A13 (1GB, 2GB)	Input	**Address inputs**: Provide the row address for ACTIVE commands and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
DM0–DM7	Input	**Input data mask**: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
DQ0–DQ63	I/O	**Data input/output**: Bidirectional data bus.
DQS0–DQS7, DQS0#–DQS7#	I/O	**Data strobe**: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SCL	Input	**Serial clock for presence-detect**: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA1	Input	**Presence-detect address inputs**: These pins are used to configure the presence-detect device.
SDA	I/O	**Serial presence-detect data**: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V_{DD}	Supply	**Power supply**: +1.8V ±0.1V.
V_{REF}	Supply	SSTL_18 reference voltage.
V_{SS}	Supply	Ground.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply**: +1.7V to +3.6V.

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Figure 2: Functional Block Diagram

S1# 10Ω
S0# 10Ω

DQS0#, DQS0, DM0 → U2, U14 (DM, CS#, DQ, DQS#)
DQ0–DQ7 → U2 DQ; U14 DQ

DQS1#, DQS1, DM1 → U6, U18 (DM, CS#, DQ, DQS#)
DQ8–DQ15 → U6 DQ; U18 DQ

DQS2#, DQS2, DM2 → U3, U13 (DM, CS#, DQ, DQS#)
DQ16–DQ23 → U3 DQ; U13 DQ

DQS3#, DQS3, DM3 → U7, U17 (DM, CS#, DQ, DQS#)
DQ24–DQ31 → U7 DQ; U17 DQ

DQS4#, DQS4, DM4 → U4, U12 (DM, CS#, DQ, DQS#)
DQ32–DQ39 → U4 DQ; U12 DQ

DQS5#, DQS5, DM5 → U8, U16 (DM, CS#, DQ, DQS#)
DQ40–DQ47 → U8 DQ; U16 DQ

DQS6#, DQS6, DM6 → U5, U11 (DM, CS#, DQ, DQS#)
DQ48–DQ55 → U5 DQ; U11 DQ

DQS7#, DQS7, DM7 → U9, U15 (DM, CS#, DQ, DQS#)
DQ56–DQ63 → U9 DQ; U15 DQ

10Ω
BA0–BA1/BA2 → BA0–BA1/BA2: DDR2 SDRAM
A0–A12 → A0–A12/A13: DDR2 SDRAM
RAS# → RAS#: DDR2 SDRAM
CAS# → CAS#: DDR2 SDRAM
WE# → WE#: DDR2 SDRAM
CKE0 → CKE0: Rank 0
CKE1 → CKE1: Rank 1
ODT0 → ODT0: Rank 0
ODT1 → ODT1: Rank 1

U1
SCL → Serial PD ↔ SDA
WP A0 A1 A2
SA0 SA1 SA2

V_{DDSPD} → Serial PD/EEPROM
V_{DD} → DDR2 SDRAM
V_{REF} → DDR2 SDRAM
V_{SS} → DDR2 SDRAM, EEPROM

Rank 0 = U2–U9
Rank 1 = U11–U18

CK0, CK0# — 100Ω, 5.6pF → U2, U3, U6, U7, U13, U14, U17, U18
CK1, CK1# — 100Ω, 5.6pF → U4, U5, U8, U9, U11, U12, U15, U16

Notes: 1. Unless otherwise noted, resistor values are 22Ω.

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General Description

The MT16HTF12864H(I) and MT16HTF25664H(I) DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 1GB and 2GB memory modules organized in x64 configuration. These DDR2 SDRAM modules use internally configured quad-bank (512Mb) or eight-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during reads and by the memory controller during writes. DQS is edge-aligned with data for reads and center-aligned with data for writes.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

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Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
VDD	VDD supply voltage relative to VSS		–1.0	+2.3	V
VDDQ	VDDQ supply voltage relative to VSS		–0.5	+2.3	V
VDDL	VDDL supply voltage relative to Vss		–0.5	+2.3	V
VIN, VOUT	Voltage on any pin relative to VSS		–0.5	+2.3	V
I_I	Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#	–80	+80	µA
		CK, CK#, S#, CKE, ODT	–40	+40	
		DM	–10	+10	
I_{OZ}	Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	–10	+10	µA
I_{VREF}	VREF leakage current; VREF = valid VREF level		–32	+32	µA
T_{CASE}	DDR2 SDRAM device operating temperature (case)[1]	Commercial	0	+85	°C
		Industrial[2]	–40	+95	°C

Notes:
1. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site at www.micron.com/technotes.
2. Refresh rate must double when T_{CASE} exceeds 85°C.

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed using simulations to close timing budgets.

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets, available on Micron's Web site. Module speed grades correlate with component speed grades as shown in Table 8:

Table 8: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-53E

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Table 9: DDR2 IDD Specifications and Conditions – 1GB
Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	80E/-800	-667	-53E	-40E	Units
Operating one bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0[1]	856	776	696	696	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1[1]	976	896	816	776	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P[2]	112	112	112	112	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q[2]	800	720	640	560	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N[2]	880	800	720	640	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating — Fast PDN Exit MR[12] = 0	IDD3P[2]	640	560	480	400	mA
Slow PDN Exit MR[12] = 1		192	192	192	192	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N[2]	1120	1040	880	720	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W[1]	1616	1416	1176	976	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R[1]	1696	1496	1216	976	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); Refresh the command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5[2]	3680	2880	2720	2640	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6[2]	112	112	112	112	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail	IDD7[1]	2456	1976	1856	1816	mA

Notes:
1. Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

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Table 10: DDR2 IDD Specifications and Conditions – 2GB (die revision A)
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[1]	856	776	696	616	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[1]	936	856	816	696	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[2]	112	112	112	112	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[2]	1040	880	656	560	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[2]	1120	960	720	640	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P[2]	720	640	560	560	mA
	Slow PDN Exit MR[12] = 1		224	224	224	224	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[2]	1200	1120	880	720	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[1]	1536	1336	1096	936	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[1]	1576	1336	1216	936	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); Refresh the command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[2]	4480	4160	4000	3520	mA
Self refresh current; CK and CK# at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[2]	112	112	112	112	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail		IDD7[1]	2736	2456	2376	2136	mA

Notes:
1. Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

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Table 11: DDR2 IDD Specifications and Conditions – 2GB (die revision E)
Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0[1]	776	736	616	616	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1[1]	936	856	816	776	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P[2]	112	112	112	112	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q[2]	800	640	640	560	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N[2]	800	640	640	560	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating — Fast PDN Exit MR[12] = 0	IDD3P[2]	640	480	480	480	mA
Slow PDN Exit MR[12] = 1		160	160	160	160	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N[2]	960	880	720	640	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W[1]	1336	1136	1056	896	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R[1]	1336	1136	1056	896	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); Refresh the command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5[2]	3760	3440	3360	3280	mA
Self refresh current; CK and CK# at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6[2]	112	112	112	112	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail	IDD7[1]	2736	2296	2216	2136	mA

Notes:
1. Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

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Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	I_{CC_R}	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	I_{CC_W}	2	3	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	KHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

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Table 14: Serial Presence-Detect Matrix
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 14

Byte	Description	Entry (Version)	MT16HTF12864H(I)	MT16HTF25664H(I)
0	Number of SPD bytes used by Micron	128	80	80
1	Total Number of bytes in SPD device	256	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08
3	Number of row addresses on assembly	14	0E	0E
4	Number of column addresses on assembly	10	0A	0A
5	DIMM height and module ranks	30mm, dual rank	61	61
6	Module data width	64	40	40
7	Module data width (continued)	0	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05
9	SDRAM cycle time, ^{t}CK (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	25 30 3D 50	25 30 3D 50
10	SDRAM access from clock,^{t}AC (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	40 45 50 60	40 45 50 60
11	Module configuration type	Non-ECC	00	00
12	Refresh rate/type	7.81µs/SELF	82	82
13	SDRAM device width (primary SDRAM)	8	08	08
14	Error-checking SDRAM data width	n/a	00	00
15	Reserved		00	00
16	Burst lengths supported	4, 8	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	08
18	CAS latencies supported	-80E (5, 4) -800 (6, 5, 4) -667 (5, 4, 3) -53E/-40E (4, 3)	30 70 38 18	30 70 38 18
19	Module thickness		01	01
20	DDR2 DIMM type	SODIMM	04	04
21	SDRAM module attributes	No PLL or Reg	00	00
22	SDRAM device attributes: Weak driver (01) and 50Ω ODT (03)	-800/-80E/-667 -53E/-40E	03 01	03 01
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	-80E/-667 -800 -53E/-40E	3D 30 50	3D 30 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-80E/-800 -667 -53E -40E	40 45 50 60	40 45 50 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-80E(N/S) -800 -667 -53E/40E(N/S)	00 3D 50 00	00 3D 50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-80E(N/S) -800 -667 -53E/-40E(N/S)	00 40 45 00	00 40 45 00

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Table 14: Serial Presence-Detect Matrix
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 14

Byte	Description	Entry (Version)	MT16HTF12864H(I)	MT16HTF25664H(I)
27	Minimum row precharge time, ^tRP	-80E -800/-667-53E/-40E	32 3C	32 3C
28	Minimum row active to row active, ^tRRD		1E	1E
29	Minimum RAS#-to-CAS# delay, ^tRCD	-80E -800/-667-53E/-40E	32 3C	32 3C
30	Minimum RAS# pulse width, ^tRAS	-800/-80E/-667/-53E -40E	2D 28	2D 28
31	Module rank density	512MB, 1GB	80	01
32	Address and command setup time, ^tIS_b	-800/-80E -667 -53E -40E	17 20 25 35	17 20 25 35
33	Address and command hold time, ^tIH_b	-800/-80E -667 -53E -40E	25 27 37 47	25 27 37 47
34	Data/data mask input setup time, ^tDS_b	-800/-80E -667/-53E -40E	05 10 15	05 10 15
35	Data/data mask input hold time, ^tDH_b	-800-80E -667 -53E -40E	12 17 22 27	12 17 22 27
36	Write recovery time, ^tWR		3C	3C
37	WRITE-to-READ command delay, ^tWTR	-80E/-667/-53E -800/-40E	1E 28	1E 28
38	Read-to-precharge command delay, ^tRTP		1E	1E
39	Memory analysis probe		00	00
40	Extension for bytes 41 and 42	-80E -800/-667/-53E/-40E	30 00	36 06
41	Minimum active auto refresh time, ^tRC (see note 1)	-80E -800/-667/-53E -40E	39 3C 37	39 3C 37
42	Minimum AUTO REFRESH to ACTIVE/ AUTO REFRESH command period, ^tRFC		69	7F
43	SDRAM device MAX cycle time, $^tCK_{MAX}$		80	80
44	SDRAM device MAX DQS-DQ skew time, ^tDQSQ	-800/-80E -667 -53E -40E	14 18 1E 23	14 18 1E 23
45	SDRAM device MAX read data hold skew factor, ^tQHS	-800/-80E -667 -53E -40E	1E 22 28 2D	1E 22 28 2D
46	PLL relock time	n/a	00	00
47–61	Optional features, not supported		00	00
62	SPD revision	Release 1.2	12	12

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Table 14: Serial Presence-Detect Matrix
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 14

Byte	Description	Entry (Version)	MT16HTF12864H(I)	MT16HTF25664H(I)
63	Checksum for bytes 0–62	-80E -800 -667 -53E -40E	92 33 4E F9 60	33 D4 EF 9A 01
64	Manufacturer's JEDEC ID code	MICRON	2C	2C
65–71	Manufacturer's JEDEC ID code	(Continued)	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C
73–90	Module part number (ASCII)		Variable Data	Variable Data
91	PCB identification code	1–9	01–09	01–09
92	Identification code (continued)	0	00	00
93	Year of manufacture in BCD		Variable Data	Variable Data
94	Week of manufacture in BCD		Variable Data	Variable Data
95–98	Module serial number		Variable Data	Variable Data
99–127	Manufacturer-specific data (RSVD)		00	00
128–255	Reserved for customer use		FF	FF

Notes: 1. The ^{t}RC SPD values shown are based on the JEDEC standard values. The actual Micron device specification is ^{t}RC = 55ns.

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Module Dimensions

Figure 3: 200-pin DDR2 SODIMM Module Dimensions

Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Revision History

Rev. B, Released (No Mark) 10/06

- Added industrial temperature components
- Added -80E speed grade
- Added -800 speed grade
- Removed redundant data that is available in the component data sheets
- Removed 512MB capacity per J. Ostberg. 512 MB capacity is available as MT8HTF6464H(I).
- Updated temperature specs
- Added CL4@533, and updated SPD to reflect the change

Rev. A, Released (No Mark) 1/06

- Removed component specifications

Rev. A, Released (No Mark) 3/05

- New data sheet (leveraged from HTF8C32_64_128X64HG)

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